REMARKS

Applicant has studied the Office Action dated August 1, 2003 and has made amendments to the claims. It is submitted that the application, as amended, is in condition for allowance. By virtue of this amendment, claims 1-4, 6-16, 25-27, and 32-38 are pending. New claims 37 and 38 have been added. Reconsideration and allowance of the pending claims in view of the above amendments and the following remarks are respectfully requested.

Claims 1-4, 6, 7, 10, 13, 25-27, 32, 33, 35, and 36 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Liao et al. (U.S. Patent No. 5,652,156) in view of Gardiner et al. (U.S. Patent No. 4,354,309) and Sakai et al. (U.S. Patent No. 4,074,300). Claim 8 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Liao et al. in view of Gardiner et al., Sakai et al., and Shih et al. (U.S. Patent No. 5,943,569). Claims 9 and 14 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Liao in view of Gardiner et al., Sakai et al., Shih et al., and Wang et al. (U.S. Patent No. 5,646,061). Claims 12, 15, 16, and 34 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Liao et al. in view of Gardiner et al., Sakai et al., and Hamasaki (U.S. Patent No. 6,274,401). These rejections are respectfully traversed.

The present invention is directed to in-situ deposition and doping methods for polycrystalline silicon layers that prevent the dopant from reaching the surface during a subsequent thermal treatment. One preferred embodiment of the present invention provides an in-situ deposition and doping method for a polycrystalline silicon layer of a semiconductor device. According to the method, a first intermediate layer of in-situ doped polycrystalline silicon is grown in a deposition chamber with a first thickness and a first doping level. After the first intermediate layer is grown, the deposition chamber is purged by stopping all gas flow into the chamber and pumping residual gas out of the chamber, so as to remove all available dopant.

After purging the deposition chamber, a second additional layer of polycrystalline silicon is grown with a second thickness and a second doping level that is lower than the first doping level. The first thickness is greater than the second thickness. Because there is provided the

thinner and less doped second layer of polycrystalline silicon, the dopant is prevented from reaching the surface during a subsequent thermal treatment. Accordingly, the present invention provides an improved method for forming an in-situ doped polycrystalline silicon layer for a semiconductor device.

The Liao reference discloses a process for forming a multilayered gate that inhibits ion penetration to the underlying gate oxide layer. The Gardiner reference discloses a process for forming a multilayer polycrystalline silicon gate that reduces void formation. However, neither Liao nor Gardiner, or a combination of the two, discloses an in-situ deposition and doping method for a polycrystalline silicon layer in which a first intermediate layer of in-situ doped polycrystalline silicon is grown with a first thickness and a first doping level, then the deposition chamber is purged by stopping all gas flow into the chamber and pumping residual gas out of the chamber so as to remove all available dopant, and then a second additional layer of polycrystalline silicon is grown with a lower second thickness and a lower second doping level, as is recited in independent claim 1. Independent claims 15, 25, and 33 contain similar recitations.

The Liao reference discloses a process for forming a multilayered gate by alternately depositing amorphous silicon layers and polycrystalline silicon layers. In particular, a first layer of amorphous silicon is deposited on an oxide layer, a second layer of polycrystalline silicon is deposited on the amorphous silicon layer, and then a third layer of amorphous silicon is deposited on the polycrystalline silicon layer. The alternating layers of amorphous silicon and polycrystalline silicon are sequentially grown such that there are mismatches in the grain boundaries between the layers in order to slow diffusion of implanted dopant during subsequent processing. Thus, Liao discloses forming a multilayer gate by depositing polycrystalline silicon layers on amorphous silicon layers so as to produce alternating layers of amorphous silicon and polycrystalline silicon.

In contrast, in embodiments of the present invention, two polycrystalline silicon layers are grown. More specifically, a first intermediate layer of in-situ doped polycrystalline silicon is

grown, then the deposition chamber is purged by stopping all gas flow into the chamber and pumping residual gas out of the chamber so as to remove all available dopant, and then a second additional layer of polycrystalline silicon is grown. Thus, in embodiments of the present invention, both the first and second layers are formed of identical polycrystalline silicon (apart from small differences induced by the different doping levels), and residual gas is pumped out of the chamber between growing these two polysilicon layers so as to remove all available dopant.

Liao does not teach or suggest growing a first polycrystalline silicon layer, then pumping residual gas out of the chamber so as to remove all available dopant, and then growing a second polycrystalline silicon layer.

With respect to growing two polycrystalline silicon layers, Liao only teaches depositing a layer of amorphous silicon on a layer of polycrystalline silicon. While Liao once states that "alternating layers of polysilicon" are formed, this does not mean that adjacent layers (i.e., both the first and second layers) can be made of polycrystalline silicon as asserted by the Examiner. To give these words the meaning asserted by the Examiner requires reading these four words alone and totally ignoring the rest of the description of Liao's invention and the purpose of Liao. These four words cannot possibly mean that the adjacent first two layers can both be formed of polycrystalline silicon. Given that the entire teaching and purpose of Liao requires the forming of a layer of amorphous silicon on an adjacent layer of polycrystalline silicon, "alternating layers of polysilicon" can only mean that there is one polysilicon layer, a layer of something else (in this case, amorphous silicon), and then another layer of polysilicon. Further, adjacent layers must include an amorphous silicon layer and a polycrystalline silicon layer, because otherwise Liao's entire purpose of exploiting the mismatch of the grain boundaries between layers to inhibit ion penetration would not be achieved.

Amorphous silicon and polycrystalline silicon are two completely different materials with different structures and properties. For example, amorphous silicon and polycrystalline silicon have different crystallographic structures, with the amorphous silicon lacking grain boundaries because it is amorphous and does not have a crystal lattice. The deposition process described in

Liao makes it completely clear that this reference does not teach suggest forming adjacent polycrystalline silicon layers.

Additionally, Liao does not state that both the first and second layers 20 and 22 "have grain boundaries" as asserted by the Examiner. Liao actually states that "[t]he mismatched grain boundaries of the gate will inhibit . . . ." This does not mean that both the first and second layers have grain boundaries. As shown in Figure 6, grain boundaries 28 are located at the interface of every two adjacent layers. Every polysilicon surface has grain boundaries and every other layer of the gate is a polycrystalline silicon layer, so passing from the first layer 20 to the second layer 22 there is a grain boundary due to the surface of the polycrystalline silicon layer at this interface (i.e., because one of the two adjacent layers, not both layers, is a polycrystalline silicon layer). Similarly, passing from the second layer 22 to the third layer 24 there is a grain boundary due to the surface of the polycrystalline silicon layer at this interface, and so on. Thus, layers are encompassed by grain boundaries, but this in no way means that two adjacent layers are the polycrystalline silicon layers.

Furthermore, while Liao states that "[t]he first layer grown may be polysilicon rather than amorphous silicon," this does not mean that Liao teaches forming both the first and second layers of polysilicon as asserted by the Examiner. To give this statement the meaning asserted by the Examiner requires reading it out of context and totally ignoring the next two sentences (not to mention the rest of the description of Liao and the entire purpose of Liao). The two sentences of Liao after the statement cited by the Examiner state: "Either polysilicon or amorphous silicon may be the top layer. The key feature of the invention is that the different types of layers alternate." Liao at 3:13-15. Further, adjacent layers must include an amorphous layer and a polycrystalline silicon layer, because otherwise Liao's purpose of exploiting the mismatch of the grain boundaries between layers to inhibit ion penetration would not be achieved. Thus, the statement cited by the Examiner actually teaches that it is possible to invert the order of the layers (i.e., to deposit a second amorphous silicon layer over a first polycrystalline silicon layer), not that both the first and second layers can be made of polycrystalline silicon.

With respect to pumping residual gas out of the chamber so as to remove all available dopant in between growing two layers, Liao only teaches turning off the gas between growing layers. Liao never teaches or suggests "pumping residual gas out of the chamber, so as to remove all available dopant" as asserted by the Examiner. Liao actually only states that "[t]he gas is turned off" in a transition from forming one layer to forming the next layer. Liao at 2:55-66.

Further, the Examiner asserts that completely removing the first gas source before introducing the second gas source merely adds complexity without providing any advantages or producing any unexpected results. This position of the Examiner is respectfully traversed.

In embodiments of the present invention, it is essential to purge the doping gas between the depositions of the first and second layers. Without this operation, the second layer would also be doped and this leads to the out-doping effects that the present invention overcomes. More specifically, "pumping residual gas out of the chamber, so as to remove all available dopant" is necessary in order to obtain large differences in the doping level of the first and second layers, and in particular to enable formation of a non-doped second layer. Such a large difference in doping levels is necessary to avoid the out-doping effect. Liao never teaches or suggests such the purging step that is necessary to remove doping gases from the deposition chamber, and thus the teaching of Liao does not make it possible to obtain the sharp doping level variations between consecutive layer that are necessary to provide the advantages of the present invention.

Accordingly, Liao does not teach or suggest the claimed features of growing two polycrystalline silicon layers or pumping residual gas out of the chamber so as to remove all available dopant in between growing two layers. Furthermore, as recognized by the Examiner, Liao does not teach or suggest growing in-situ doped polycrystalline silicon layers, that the doping level of the second layer is lower than the doping level of the first layer, or that the thickness of the first layer is greater than the thickness of the second layer.

The Gardiner reference adds to the teaching of Liao that two layers of polysilicon can be in-situ doped with different doping levels. However, Gardiner teaches depositing <u>increasingly</u>

doped layers of polycrystalline silicon. In particular, a first intrinsic (non-doped) layer of polycrystalline silicon is deposited, a second moderately doped layer of polycrystalline silicon is deposited, and then a third strongly doped layer of polycrystalline silicon is deposited. The dopant is then diffused through the three layers by subsequent thermal processes. The three layers all have the same thickness (1000 Å), so the resulting average doping level is approximately 1/3 of the doping of the strongly doped third layer. Thus, Gardiner discloses forming a multilayer gate by depositing three polycrystalline silicon layers having the same thicknesses but with doping levels that increase in the order of deposition.

In contrast, in embodiments of the present invention, the thickness of the first layer is greater than the thickness of the second layer, and the doping level of the second layer is lower than the doping level of the first layer. Thus, in embodiments of the present invention, a first polycrystalline silicon layer is formed, and then a thinner and less doped second polycrystalline silicon layer is formed.

Gardiner does not teach or suggest growing a first polycrystalline silicon layer, and then growing a thinner and less doped second polycrystalline silicon layer. While Gardiner may generally disclose that it is possible to deposit in-situ doped polycrystalline silicon layers having different doping levels, Gardiner specifically teaches a process in which the second layer has a greater doping level than the first layer, and the third layer has a greater doping level than the second layer. In other words, Gardiner teaches that each layer of polycrystalline silicon is deposited with a higher doping level than the previously-deposited layers. Thus, Gardiner actually teaches away from the claimed feature of growing a second polycrystalline silicon layer that is less doped than the previously-grown layer. The Examiner cannot make out a case of obviousness by altering the teachings of Gardiner so as to include a feature that is specifically taught away from by the reference itself. Further, if the process of Gardiner is altered so that a less-doped polycrystalline silicon layer is deposited over a higher-doped polycrystalline silicon layer, then Gardiner's purpose of reducing void formation in the lower layer so as to inhibit degradation of the underlying gate oxide layer during subsequent processing would not be achieved. The Examiner cannot altering the process disclosed in Gardiner so as to render it unsatisfactory for its intended purpose or change it principle of operation.

The Sakai reference may disclose forming two polysilicon layers having different doping levels, with the doping level of the second layer is lower. However, it is improper to combine these three references because Sakai and Gardiner teach opposing doping levels for the two polycrystalline silicon layers. As explained above, Gardiner specifically teaches a process in which each layer of polycrystalline silicon is deposited with a higher doping level than the previously-deposited layers. Thus, Sakai and Gardiner have opposing teachings, and Gardiner actually teaches away from the claimed invention. The Examiner cannot make out a case of obviousness by combining references with opposing teachings because this would require one of the reference's teaching to be altered so as to include a feature that is specifically taught away from by the reference itself and that would render it unsatisfactory for its intended purpose or change it principle of operation.

Accordingly, none of Liao, Gardiner, and Sakai, or a combination of the three, teaches or suggests the claimed features of the present invention.

The Examiner also took the position that it would be a matter of routine optimization by one of ordinary skill in the art to choose particular thicknesses and doping levels because such depend on the desired device characteristics and dimensions. This position of the Examiner is respectfully traversed.

The claimed relative thicknesses and doping levels recited in the claims of the present invention are not merely optimized for a specific application from the general teachings of the cited references or any other reference. This is not a case of optimization of known teachings for a specific purpose, but is instead a novel solution to the well known problem described in the background section of the specification. This is made clear by the fact that the claimed features are a less in-situ doped and thinner second layer, while the cited references respectively teach non in-situ doped layers and increasingly doped layers, along with same thickness layers or increasing thickness layers. The claimed features simply cannot be mere routine optimizations of known characteristics and dimensions when the claimed features go in a different direction than the characteristics and dimensions that are taught.

Further, these claimed characteristics and dimensions are necessary to provide the advantages of the present invention. In particular, a thinner and less doped second polycrystalline silicon layer is required to prevent the dopant from reaching the surface during subsequent thermal treatment. The cited references do not overcome the problems described in the background section of the specification and fail to provide such an advantage. Thus, it is improper for the Examiner to say that the recited characteristics and dimensions are matters of routine optimization, and the Examiner must instead use what is actually disclosed in the prior art itself to show that the claimed invention was taught or suggested by the prior art in order to properly reject claims. The Examiner cannot just state that any features missing from the prior art are "maters of routine optimization". If such features are known and merely routine choices, then the Examiner should have no problem finding at least one prior art reference that teaches the general concept and does not teach away from the present invention.

Likewise, the Examiner cannot say that thicknesses and doping levels are always result effective variables and always just a matter of determining optimum process conditions by routine experimentation. In this case, the present invention changed the entire process and produced unexpected results. As explained in the specification, the current trend in forming polysilicon gate layers is to use an in-situ doping technique in which a polysilicon layer is both grown and doped at the same time, but this causes several problems due to the high doping levels that need to be reached such as the occurrence of the out-doping effect. The present invention overcomes the out-doping effect, and this is an unexpected result that is different in kind and not in just in degree from the processes (including all thickness and doping values) in the cited references. None of the cited references is aimed at, or produces, a solution to this problem.

In particular, out-doping is overcome according to the present invention by forming a first doped layer of polysilicon, then purging the first gas mixture from the deposition chamber, and then forming a second polysilicon layer which is less doped and thinner. The second polysilicon layer must be less doped (e.g., non-doped) and thinner (e.g., by a ratio of 1:10) than the first layer to produce these advantages. This is because the thickness of the second less doped layer determines the average doping level of the two layers once the redistribution of doping atoms takes place, and a significant change in the first layer doping level is not wanted. Thus, as

explained in the specification, it is necessary to have a second less layer that is thinner than the first layer to achieve the desired and advantageous results. This is not merely a simple optimization of the second layer thickness and doping level that can be achieved through routine experimentation of the processes in the cited references, but instead the result is very different in kind and degree from the results of the cited references.

Furthermore, Applicant submits that it is improper to combine these three (or more) references to each show individual process features of the claimed invention. The use of all of these different references for each individual process feature demonstrates that the combination of claimed process features is not obvious.

Additionally, even if the cited references each suggest one or more individual features of the invention, there is no teaching or suggestion to simultaneously use all of the claimed features in a single process. The Examiner has not cited any reference or generally available knowledge that suggests or provides any motivation for combining the individual claimed process features so as to produce the claimed process as it is recited.

Nearly all integrated circuit fabrication processes include the same basic steps (such as depositing layers, doping layers, and etching layers) combined in different manners with very different results. If all that was required to sustain a finding of obviousness was that each separate feature of an integrated circuit fabrication process was disclosed in some other process, then few (if any) integrated circuit fabrication process patents would be issuing at this time. However, a great number of such patents continue to issue because this is certainly not the law and there must be shown some specific motivation for combining a process feature found in one reference in a specific manner into a different type of fabrication process found in another reference in order to sustain a finding of obviousness. Here, the specific arrangement of the recited process features makes it possible to overcome the out-doping effect.

Additionally, an individual process feature found in one reference cannot simply be substituted into a different type of circuit structure in another reference with the same results. Even a small change in the type and timing of a specific process feature in relation to other

process features can produce very different and unexpected results. None of the cited references provides any suggestion or motivation for performing the process as recited.

The cited references fail to meet the basic requirement for a finding of obviousness established by the courts. There is simply no suggestion or motivation in any of these references for combining selected features of one reference with the fabrication process of the other reference in order to produce a single fabrication process, nor is there any suggestion of the desirability of such a combination. Without the knowledge gleaned from Applicant's specification, there would be no suggestion or motivation to one of ordinary skill in the art at the time of the invention to produce the recited fabrication process. It is respectfully submitted that the Examiner is engaging in improper hindsight reconstruction of the claimed invention.

Applicant believes that the differences between the Liao, Gardiner, Sakai, and the present invention are clear in independent claims 1, 15, 25, and 33, which set forth in-situ deposition and doping methods according to various embodiments of the present invention. Therefore, claims 1, 15, 25, and 33 distinguish over the Liao, Gardiner, and Sakai references, and the rejections of these claims under 35 U.S.C.§ 103(a) should be withdrawn.

As discussed above, claims 1, 15, 25, and 33 distinguish over the Liao, Gardiner, and Sakai references. Furthermore, the claimed features of the present invention are not realized even if the teachings of Shih, Wang, and Hamasaki are incorporated into Liao, Gardiner, and Sakai. None of Shih, Wang, and Hamasaki teaches or suggests the claimed features of the present invention that are absent from Liao, Gardiner, and Sakai. Thus, claims 1, 15, 25, and 33 distinguish over the Liao, Gardiner, Sakai, Shih, Wang, and Hamasaki references, and thus, claims 2-4, 6-10, 12-14, and 27, claim 16, claims 26 and 32, and claims 34-36 (which depend from claims 1, 15, 25, and 33, respectively) also distinguish over the Liao, Gardiner, Sakai, Shih, Wang, and Hamasaki references. Therefore, it is respectfully submitted that the rejections of claims 1-4, 6-10, 12-16, 25-27, and 32-36 under 35 U.S.C. § 103(a) should be withdrawn.

Applicant notes that claim 11 was not rejected. Accordingly, it is submitted that claim 11 is in condition for allowance.

Claims 37 and 38 have been added by this amendment, and are provided to further define the invention disclosed in the specification. Claims 37 and 38 are allowable for at least the reasons set forth above with respect to claims 1-4, 6-16, 25-27, and 32-36.

In view of the foregoing, it is respectfully submitted that the application and the claims are in condition for allowance. Reexamination and reconsideration of the application, as amended, are requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is invited to call the undersigned attorney at (561) 989-9811 should the Examiner believe a telephone interview would advance the prosecution of the application.

Respectfully submitted,

Date: February 2, 2004

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